REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 7-33. Specifically, the Office Action rejected claims 7-33 under 35 U.S.C. 102(b), as being anticipated by Rajeevakumar (U.S. 5,426,324). Applicants have amended claims 13 and 25. No new matter has been added to the application by the amendments made to the claims or otherwise in the application. Reconsideration and withdrawal of the Examiner's rejection is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 7-33 under 35 U.S.C. 102(e), as being anticipated by Rajeevakumar (U.S. 5,426,324). Applicants respectfully traverse the rejections for at least the reasons set forth below.

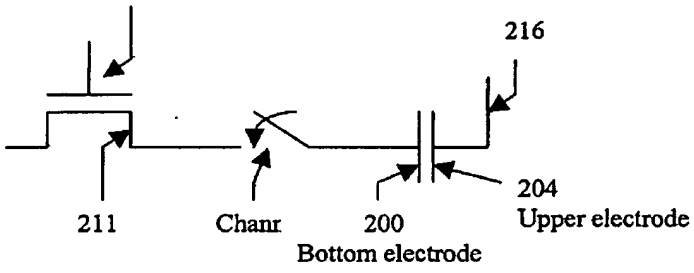
To anticipate a claim, the reference must teach each and every element of the claim. M.P.E.P. § 2131

Applicants respectfully assert that Rajeevakumar is legally deficient for the purpose of anticipating claims 7, 13, 18 and 25 for at least the reason that not every element of the claim was taught or suggested by cited references.

The present invention specifically teaches "said conducting layer ***being an upper electrode***, said substrate around said capacitor dielectric layer ***being a bottom electrode***." as recited in claims 7 and 18 or "said substrate around said first and second capacitor dielectric layers ***being a bottom electrode***", "a second capacitor dielectric layer between said protruding electrode and said substrate" and "said conducting layer, and said conducting layer, said protruding electrode, and said conducting structure ***being an upper electrode***" as recited in claims 13 and 25.

The present invention is directed to a DRAM cell. The DRAM cell, as shown in FIG. 2H and diagram below, comprises a capacitor including a substrate 200, a conducting layer 204, conducting structure 216, protruding electrode 208a, a dielectric layer 202 and a dielectric layer

206a and a transistor including a gate electrode 208b, a source/drain region 211 and a gate dielectric layer 206b. The conducting layer 204 and protruding electrode 208a connect to the conducting structure 216 to serve as an upper electric electrode of the capacitor. An inversion layer is formed in the channel under the protruding electrode 208a when a voltage is applied on the protruding electrode 208a through the conducting structure 216. Thereby, the inversion layer connects the source/drain 211 and the substrate 200, and the substrate 200 around the dielectric layer 2 serves as a bottom electrode of the capacitor.



However, Rajeevakumar does not teach that the trench poly node 11, the gate poly 2 and the contact 8 serve as an upper electric electrode of the capacitor and the substrate 1 around the dielectric layer 10 serves as a bottom electrode. In Rajeevakumar, FIG. 8a is a middle step diagram and is not a complete final structure. FIG. 8a does not show a contact connect to the gate poly 2 to apply a voltage thereon to form a inversion layer under the gate poly 2 in the substrate 1. Therefore, the gate poly 2 and the trench poly node 11 are not an upper electrode and the substrate around the dielectric layer 10 is not a bottom electrode. In fact, FIG. 1 is still a final structure diagram. As shown in FIG. 1, the region between the collars 31 and diffusion region 13 is not a channel since it is doped with boron to extend the diffusion region 13. Furthermore, a hole 35 is formed and a contact 8 is formed in the hole 35 to contact the diffusion region 13. Specifically, Rajeevakumar, as shown in FIG. 1, indicates that there is no dielectric layer between the contact 8 and substrate as well as the trench poly node 11 and the gate poly 2 connect to the diffusion region 13 through the contact 8. Therefore, the trench poly node 11 and the gate poly 2 serve as a bottom electrode and the substrate 1 serve as an upper electrode. In other words, the

trench poly node 11, the gate poly 2 and the contact 8 are not equivalent to the conducting layer 204, protruding electrode 208a and the conducting structure 216 of the present invention, respectively.

Therefore, neither claim 7 nor claims 13, 18 and 25 is anticipated by Rajeevakumar since the Rajeevakumar does not disclose each and every element of the claims. Applicant notes that Examiner has also rejected claims 8-12, 14-17, 19-24 and 26-33 and Applicant respectfully disagrees with the Examiner's statements. Since claims 8-12, 14-17, 19-24 and 26-33 are respectively dependent upon claims 7, 13, 18 and 25, which are not anticipated by Rajeevakumar, claims 7, 13, 18 and 25 are consequently not anticipated by Rajeevakumar.

For at least the foregoing reasons, Applicants respectfully submit that the grounds of rejections have been addressed and the rejections overcome. Reconsideration and withdrawal of the rejections are respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 7-33 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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